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GARLICK HARRISON & MARKISON LLP
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,984	YEH ET AL.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-16,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-16,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6, 9-16 and 19-20 have been examined.

2. Acknowledgement of papers filed: amendment filed on 9/23/2005.

New Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 20 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 20 is for "A carrier medium comprising one or more data structures representing a processor." A "carrier medium" does not fall within any of the categories of patentable subject matter set forth in § 101, since it has been defined in the specification (pages 52-53) to include nonstatutory "transmission media or signals such as electrical, electromagnetic, or digital signals, conveyed via a communication medium such as a network and/or a wireless link." See at least pages 55-57 of "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility," herein referred to as "Interim Guidelines," which can be found on the USPTO website at http://www.uspto.gov/web/offices/pac/dapp/ogsheet.html for further information. Specifically, page 55, 1st full paragraph states, "it does not appear that a claim reciting a signal encoded with function descriptive material falls within any of the categories of patentable subject matter set forth in § 101.

Maintained Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-5 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Avnon et al., U.S. Patent 5,559,977, herein referred to as Avnon. (Examiner notes that the heading was left incomplete in the last Final Office Action because it was lacking claim 11, however, claim 11 was rejected under 102(b) as being anticipated by Avnon in the Final Office Action, and therefore the Maintained 35 USC 102 Rejection to claim 11 is not a new rejection.)

7. As per claim 1, Avnon teaches a processor comprising:

-A first pipeline having a first number of stages to process instructions: (Integer pipeline, depicted in figure 4, IP3 and IP4. Column 7, lines 50-59)

-A second pipeline having a second number of stages, which is greater than the first number of stages, to process floating point instructions: (Floating Point pipeline, column 7, lines 35-65. Figure 4, IP1 and IP2)

-And a control circuit coupled to the first and second pipelines to inhibit co-issuance of a first instruction to the first pipeline, if a second instruction to be issued to the second pipeline is a floating point instruction and the first instruction is subsequent to the second instruction in program order: (The microvector

sequencers 104u and 104v (figure 1) control the stalling of instructions issuance to both the integer and floating point pipelines. (Column 6, lines 51-65). This occurs when a second instruction (a floating point instruction within a pair of floating-point instructions) is determined to be a part of a pair of floating-point instructions that are unsafe. All subsequent integer instructions are stalled and not co-issued to the execution unit, which they otherwise would be, as two integer instructions can be co-issued under normal circumstances. For the issuing inhibiting see column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. For normal issuing see figure 3, column 6, lines 30-39 and column 7, lines 22-3)

-The first instruction to be inhibited for a predetermined number of stage cycles until the first instruction is determined not to graduate from the first pipeline at least no earlier than the second instruction reaching a stage in the second pipeline where exceptions are to be generated to ensure that the first instruction does not graduate from the first pipeline prior to exception determination for the second instruction in the second pipeline: (Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. The subsequent integer instructions are not co-issued until the second instruction (unsafe floating point instruction within an unsafe floating point instruction pair) is deemed safe or it is handled.)

8. As per claim 3, Avnon teaches the processor as recited in claim 1, wherein the second instruction is a long latency floating point instruction. (The floating point

instructions have a longer latency then the integer instructions as shown by the two different pipelines utilized (see figure 4 and column 7, lines 35-59). Therefore, the second instruction as described in regard to claim 1 above is a long latency floating point instruction.)

9. Given the similarities between claim 3 and claim 13, the arguments as stated for the rejection of claim 3 also apply to claim 13.

10. As per claim 4, Avnon teaches the processor as recited in claim 1, wherein the first instruction is an integer instruction and the first pipeline is an integer pipeline. (The integer pipeline is depicted in figure 4, IP3 and IP4 and column 7, lines 50-59. The first instruction is an integer instruction as described in regard to claim 1 above.)

11. Given the similarities between claim 4 and claim 14, the arguments as stated for the rejection of claim 4 also apply to claim 14.

12. As per claim 5, Avnon teaches the processor in claim 1, wherein the first instruction is a load/store instruction and the first pipeline is a load/store pipeline: (Column 4, lines 27-65 and column 1, line 57 to column 2, line 2. The execution units 105u and 105v and address generators 106u and 106v, are part of the integer pipeline, and execute load/store instructions, and therefore it is also a load/store pipeline.)

13. Given the similarities between claim 5 and claim 15, the arguments as stated for the rejection of claim 5 also apply to claim 15.

14. As per claim 11, Avnon teaches a method comprising:

-Queuing a first instruction for issuance to a first pipeline having a first number of stages: (Integer pipeline, depicted in figure 4, IP3 and IP4. Column 7, lines 50-59)

-Queuing a second instruction, which is a floating point instruction, for issuance to a second pipeline having a second number of stages, which is greater than the first number of stages, to process floating point instructions: (Floating Point pipeline, column 7, lines 35-65. Figure 4, IP1 and IP2)

-Issuing the second instruction to the second pipeline: (Floating Point instructions are issued to the second pipeline, column 7, lines 35-65. Figure 4, IP1 and IP2)

-And inhibiting co-issuance of the first instruction to the first pipeline if the first instruction is subsequent to the second instruction in program order, (The microvector sequencers 104u and 104v (figure 1) control the stalling of instructions issuance to both the integer and floating point pipelines. (Column 6, lines 51-65). This occurs when a second instruction (a floating point instruction within a pair of floating-point instructions) is determined to be a part of a pair of floating-point instructions that are unsafe. All subsequent integer instructions are stalled and not co-issued to the execution unit, which they otherwise would be, as two integer instructions can be co-issued under normal circumstances. For the issuing inhibiting see column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. For normal issuing see figure 3, column 6, lines 30-39 and column 7, lines 22-3)

-The first instruction to be inhibited for a predetermined number of stage cycles until the first instruction is determined not to graduate from the first pipeline at least no earlier than the second instruction reaching a stage in the second pipeline where exceptions are to be generated to ensure the that the first instruction does not graduate from the first pipeline prior to exception determination for the second instruction in the second pipeline: (Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. The subsequent integer instructions are not co-issued until the second instruction (unsafe floating point instruction within an unsafe floating point instruction pair) is deemed safe or it is handled.)

15. As per claim 20, given the similarities between claim 1 and claim 20, the arguments as stated for the rejection of claim 1 also apply to claim 20.

Maintained Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 2, 9-10,12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avnon et al., U.S. Patent 5,559,977, herein referred to as Avnon, in view of Hennessy and Patterson, Computer Architecture, A Quantitative Approach.

18. As per claim 2, Avnon teaches the processor as recited in claim 1, however fails to further teach wherein the control circuit can disable generation of exceptions.

19. However, Patterson teaches wherein floating point exceptions are user maskable, and therefore it is possible to disable the generation of exceptions. Since handling exceptions can be costly to processing speed because of the context saving, actual handling, and restarting of the instructions, one of ordinary skill in the art would have recognized that it can be beneficial to selectively disable certain exceptions. Since the microvector sequencers handle portions of exception handling, and the ability to selectively disable exceptions is a desirable function in a processor, it would have been obvious to one of ordinary skill in the art to add the functionality of disabling exception generation to the control circuit of the processor. (Pages 180-183)

20. Given the similarities between claim 2 and claim 12, the arguments as stated for the rejection of claim 2 also apply to claim 12.

21. As per claim 9, the processor as recited in claim 1, however fails to further teach the processor comprising a scoreboard coupled to the control circuit and the scoreboard includes a set of scoreboard registers to maintain scoreboarding of pending reads and writes.

22. However, Patterson has taught a scoreboard scheme in a superscalar processor to track the data dependencies between instructions in a processor [page 242-251] since "if two instructions are data dependent they cannot execute simultaneously or be completely overlapped" [page 230]. The scoreboard would allow the tracking of register writes, allowing for the data dependencies to be tracked. Inhibiting instruction issuing

when there are register writes ensures correct instruction execution since there is no chance a depending instruction will read the register before it is written. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor of Halfhill to include a scoreboard to maintain scoreboarding of pending reads and writes.

23. Given the similarities between claim 9 and claim 19, the arguments as stated for the rejection of claim 9 also apply to claim 19.

24. As per claim 10, the processor as recited in claim 9 wherein the scoreboard uses bits for scoreboard registers to indicate that a write is pending. (The scoreboard has an entry with registers (source/destination) for every pending instruction, including writes, and indicates each instruction's status. (See pages 246-247 of Patterson) It is inherent that bits are used to indicate the data within entries of the scoreboard table because it is for a digital processor.)

25. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avnon et al., U.S. Patent 5,559,977, herein referred to as Avnon in view of Halfhill, "SiByte Reveals 64-Bit Core for NPUs."

26. As per claim 6, Avnon teaches the processor in claim 1, however fails to specifically teach wherein one of the floating point instructions is a floating point multiply-add instruction, and therefore fails to teach wherein the second instruction is a floating point multiply-add instruction:

27. Given the similarities between claim 6 and claim 16, the arguments as stated for the rejection of claim 6 also apply to claim 16.

28. Halfhill teaches wherein a floating point execution unit executes floating point multiply-add instructions. One of ordinary skill in the art would have recognized that adding the capability of a multiply-add instruction would advantageously expand the functionality of the floating point execution unit. The added functionality would have provided one of ordinary skill in the art with the motivation to add the multiply-add instruction to the possible floating point instructions that care executable by the floating point execution unit. This would in turn cause the second instruction to be a floating point multiply-add instruction in some instances.

Response to Arguments

1. Applicants arguments filed on 9/23/2005 have been fully considered but they are not persuasive.

2. Applicant argues the novelty/rejection of claim 1 (and presumably claims 11 and 20 as well).

"Applicant submits that Avnon fails to disclose the claimed embodiments of the invention...The Examiner has noted a number of lines of text in Avnon in presenting his reasons for rejecting the pending claims. ***However, the teachings of Avnon pertain to a single pipeline structure***. For example, Figure 3 of Avnon illustrates four stages of a pipeline for integer instructions handling, so that 'instruction pairs (i.e., IP1-4) being executed in the D1, D2, E and WB stage in synchronization' (Avnon at col. 7, lines 22-23). The floating-point pipeline 'shares the first four stages with the integer pipeline and then continues with four more stages X1, X2, WF and ER' (Avnon at col. 7, lines 35-38). In Figure 4 of Avnon, 'IP1 and IP2 are floating-point instructions while IP3 and IP4 are integer instruction pairs' (Avnon at col. 7, lines 50-51)." (Emphasis added by Examiner)

"***Applicant submits that the claimed embodiments of the invention pertain to multiple pipelines (first and second pipelines in claim 1) and not to a single shared pipeline.*** With multiple pipelines, an instruction to the pipelines with less stages is inhibited form co-issuing to that pipeline. This applies to a single floating-point instruction being issued to the pipeline having greater number of stages, in which co-issuing of an instruction to the shorter pipeline is inhibited. Applicant submits that these aspects of the invention as claimed in the

independent claims are not disclosed by Avnon or any of the other relied upon references." (Emphasis added by Examiner)

3. These arguments are not found persuasive for the following reasons:

a. To clarify, Examiner agrees and acknowledges the Integer and Floating-Point pipelines, do share pipeline stages, however, this does not preclude the existence of two pipelines and necessitate a single pipeline. Avnon teaches that the Floating Point pipeline shares the first four stages of the Integer Pipeline, which looking at figure 4, consists of the PF, D1, D2 and E stages. The Integer Pipeline consists of five stages, PF, D1, D2, E and WB, while the Floating-Point Pipeline consists of stages, PF, D1, D2, E, X1, X2, WF, and ER. The Integer Pipeline contains a stage that the Floating-Point Pipeline does not (the WB stage) and the Floating-Point Pipeline contains stages that the Integer Pipeline does not (the X1, X2, WF, and ER). Therefore, the two pipelines are in fact distinct, separate pipelines, which share some pipeline stages.

b. Furthermore, Examiner respectfully notes that the paragraph between pages 5-6 of the Remarks section contains a series of quotes from the specification of Avnon, without any explicit reasons as to why they support the "single pipeline" argument, and the reasons do not appear self-evident to Examiner. In fact, the cited portions explicitly state that there is a floating-point pipeline that stalls a co-issuance of an integer instruction that is in the D2 stage (which is a portion of the integer pipeline).

c. Furthermore, Applicant's claimed invention also shares pipeline stages. The specification and figures show that the Integer Pipeline shares the

Fetch/Decode/Issue Unit 14 with the Floating-Point Pipeline (Fig. 1, page 5, and lines 16-30. Therefore, if sharing pipeline stages is the criteria for classifying a pipeline as a "single pipeline," Applicant's claimed invention also falls under that same classification, and then the invention of claim 1 would not be properly enabled since there would only be one disclosed pipeline.

Conclusion

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100